ABSTRACT

Methods and apparatus are provided for processing variable width instructions in a pipelined processor. The apparatus includes an instruction decoder configured to decode a loop setup instruction, having a loop setup instruction address, to obtain a loop bottom offset and configured to decode instructions following the loop setup instruction, each having an instruction address, to obtain an instruction width, registers for holding the loop setup instruction address and the loop bottom offset, and a loop bottom detector, responsive to a current instruction address, a current instruction width, the loop setup instruction address and the loop bottom offset, configured to determine if a next instruction is a loop bottom instruction.